

Electronic Acknowledgement Receipt

EFS ID:	1058345
Application Number:	10734708
Confirmation Number:	2373
Title of Invention:	Method for fabricating transistor gate structures and gate dielectrics thereof
First Named Inventor:	Mark R. Visokay
Customer Number:	23494
Filer:	Jacqueline J. Garner./Marianna Smith
Filer Authorized By:	Jacqueline J. Garner.
Attorney Docket Number:	TI-35227
Receipt Date:	25-MAY-2006
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Application Type:	Utility
International Application Number:	

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part	Pages
1	Letter to Official Draftsman Filed P/E	T35227_Formal_Drawings_Trans_jjg.pdf	2665	no	1

Warnings:**Information:**

2	Drawings	T35227-Formal_Drws.pdf	343751	no	5
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Warnings:**Information:**

Total Files Size (in bytes):	346416
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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.